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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/520,079	08/28/1995	SHUNPEI YAMAZAKI	740756-001400	1321

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EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

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04/02/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	08/520,079	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *87,88,90,123,124 and 126* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *87,88,90,123,124 and 126* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 1995* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/17/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Supplemental Amendment filed December 17, 2009.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 87, 88 and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura (US 5,534,716).

Regarding claims 87, 88 and 90, Takemura discloses a semiconductor device (Fig. 4F) comprising a first thin film transistor (transistor formed in region 111 shown in Fig. 4C) provided in a matrix pixel circuit (col. 6, lines 12 and 49) over a substrate (101) (col. 6, line 16), and a second thin film transistor (transistor comprising gate 115 in region 110) provided in a peripheral driving circuit (col. 6, lines 10-12 and 48-49) over the substrate (101), each of the first and second thin film transistors comprising a crystalline semiconductor island (106 and 107 in Figs. 4B and 5A) (col. 6, lines 30 and 42-43), source and drain regions (portions of 118 and 119) (col. 7, line 67 - col. 8, line 2) in the crystalline semiconductor island (106 and 107), a channel forming region between the source and drain regions (portions of 118 and 119), a gate insulating film (portion of layer 113 in Fig. 4D) (col. 7, line 35) adjacent to at least the channel forming region, and a gate electrode (115 and 116) (col. 7, line 37) adjacent to the channel forming region

having the gate insulating film (portion of layer 113) therebetween, wherein each of the crystalline semiconductor islands (106 and 107) of the first and second thin film transistors is formed in a monodomain region (106 and 107) which contains no grain boundary shown in Figs. 7 and 12A of current Application, wherein the crystalline semiconductor island (107) of the first thin film transistor (transistor formed in region 111) and the crystalline semiconductor island (106) of the second thin film transistor (transistor comprising gate 115) include nickel at a concentration of about 10^{17} to 10^{20} cm^{-3} (col. 6, lines 63-64) (claim 87), wherein each of the crystalline semiconductor islands (106 and 107) of the first and second thin film transistors comprises Ni (claim 88), and each of the crystalline semiconductor islands (106 and 107) of the first and second thin film transistors is a silicon island (claim 90).

Takemura further discloses that annealing of the semiconductor device (Fig. 4F) is conducted in a hydrogen atmosphere to complete the semiconductor device (col. 8, lines 12-14), amount of nickel added may be in a range of 1×10^{17} to 1×10^{20} cm^{-3} (col. 2, lines 47-50), and high nickel concentration regions may have a nickel concentration about one order higher than in a crystallized region (col. 6, lines 55-57).

Takemura differs from the claimed invention by not showing that at least one of hydrogen and halogen element is contained at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain regions of the first and second thin film transistors, wherein the crystalline semiconductor island of the second thin film transistor includes nickel at a concentration of 1×10^{17} to 5×10^{17} cm^{-3} and the crystalline semiconductor island of the first thin film transistor includes nickel at a concentration of 1×10^{16} cm^{-3} or less.

It would have been obvious, if not inherent, to one of ordinary skill in the art at the time the invention was made that hydrogen is contained at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain regions of the first and second thin film transistors due to contamination during deposition of the semiconductor layer and annealing in a hydrogen environment, because hydrogen is a common contaminant during a semiconductor processing in an air ambient or vacuum, and can diffuse through insulating or metal layers. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the crystalline semiconductor islands of the first and second thin film transistors may include nickel at a concentration in the claimed ranges especially when amount of nickel added is about 1×10^{17} cm^{-3}, because a concentration of nickel may be controlled to form a high quality crystalline semiconductor island, while reducing adverse effects caused by nickel, there is a variation of a nickel concentration in the crystalline semiconductor islands, and Applicants do not specifically claim a range of an *average* or a *uniform* nickel concentration. Further regarding claim 87, the claim is *prima facie* obvious without showing that the claimed ranges of the hydrogen and nickel concentrations achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in

known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

3. Claims 123, 124 and 126 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura (US 5,534,716) in view of Zhang et al. (US 5,403,772).

Regarding claims 123, 124 and 126, Takemura discloses a semiconductor device (Fig. 4F) comprising a first thin film transistor (transistor formed in region 111) provided in a matrix pixel circuit (col. 6, lines 12 and 49) over a substrate (101) (col. 6, line 16), and a second thin film transistor (transistor comprising gate 115 in region 110) provided in a peripheral driving circuit (col. 6, lines 10-12 and 48-49) over the substrate (101), each of the first and second thin film transistors comprising a crystalline semiconductor island (106 and 107 in Figs. 4B and 5A) (col. 6, lines 30 and 42-43), source and drain regions (portions of 118 and 119) (col. 7, line 67 - col. 8, line 2) in the crystalline semiconductor island (106 and 107), a channel forming region between the source and drain regions (portions of 118 and 119), a gate insulating film (portion of layer 113) (col. 7, line 35) adjacent to at least the channel forming region, and a gate electrode (115 and 116) (col. 7, line 37) adjacent to the channel forming region having the gate insulating film (portion of layer 113) therebetween, wherein each of the crystalline semiconductor islands (106 and 107) of the first and second thin film transistors is formed in a monodomain region (106 and 107) which contains no grain boundary shown in Figs. 7 and 12A of current Application, wherein the crystalline semiconductor island (107) of the first thin film transistor (transistor formed in region 111) and the crystalline semiconductor island (106) of the second thin film transistor

(transistor comprising gate 115) include nickel at a concentration of about 10^{17} to 10^{20} cm^{-3} (col. 6, lines 63-64) (claim 123), wherein each of the crystalline semiconductor islands (106 and 107) of the first and second thin film transistors comprises Ni (claim 124), and each of the crystalline semiconductor islands (106 and 107) of the first and second thin film transistors is a silicon island (claim 126).

Takemura further discloses that annealing of the semiconductor device (Fig. 4F) is conducted in a hydrogen atmosphere to complete the semiconductor device (col. 8, lines 12-14), amount of nickel added may be in a range of 1×10^{17} to 1×10^{20} cm^{-3} (col. 2, lines 47-50), and high nickel concentration regions may have a nickel concentration about one order higher than in a crystallized region (col. 6, lines 55-57).

Takemura differs from the claimed invention by not showing that each of the crystalline semiconductor islands of the first and second thin film transistors includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}, and each of the crystalline semiconductor islands of the first and second thin film transistors includes at least one of hydrogen and halogen element at concentration not higher than 1×10^{20} cm^{-3} in the monodomain region, wherein the crystalline semiconductor island of the second thin film transistor includes nickel at a concentration of 1×10^{17} to 5×10^{17} cm^{-3} and the crystalline semiconductor island of the first thin film transistor includes nickel at a concentration of 1×10^{16} cm^{-3} or less.

It would have been obvious, if not inherent, to one of ordinary skill in the art at the time the invention was made that hydrogen is contained at a concentration not higher than 1×10^{20} cm^{-3} in the monodomain region due to contamination during deposition of

the semiconductor layer and annealing in a hydrogen environment, because hydrogen is a common contaminant during a semiconductor processing in an air ambient or vacuum, and can diffuse through insulating or metal layers. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the crystalline semiconductor islands of the first and second thin film transistors may include nickel at a concentration in the claimed ranges, because a concentration of nickel may be controlled to form a high quality crystalline semiconductor island, while reducing adverse effects caused by nickel, and there is a variation of a nickel concentration in the crystalline semiconductor islands, and Applicants do not specifically claim a range of an *average* or a *uniform* nickel concentration.

Further regarding claim 123, Takemura differs from the claimed invention by not showing that each of the crystalline semiconductor islands of the first and second thin film transistors includes carbon and nitrogen at a concentration not higher than 5×10^{18} cm^{-3}.

Zhang et al. disclose a semiconductor device (Fig. 8(A)) comprising a matrix pixel circuit (103) (col. 9, line 61) and a peripheral driving circuit (101 or 102) (col. 9, line 60), wherein a concentration of carbon, nitrogen and oxygen in the active layer is desirable to be less than 1×10^{18} cm^{-3} (col. 9, line 67 - col. 10, line 3).

Since both Takemura and Zhang et al. teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that concentrations of carbon and nitrogen in the crystalline semiconductor islands

disclosed by Takemura may be within the claimed ranges, because concentrations of carbon and nitrogen can be controlled to achieve a desired mobility.

Further regarding claim 123, the claim is *prima facie* obvious without showing that the claimed ranges of carbon, nitrogen, hydrogen and nickel concentrations achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Response to Arguments

4. Applicants' arguments filed October 16, 2009 have been fully considered but they are not persuasive.

Applicants argue that "however, the subject matter of Takemura is disqualified as prior art in accordance with the MPEP 706.02(l)(3) for examination procedure with respect to 35 U.S.C. 103(c)". MPEP 706.02(l) clearly stipulates that "[F]or applications filed prior to November 29, 1999 and granted as patents prior to December 10, 2004, the subject matter that is disqualified as prior art under 35 U.S.C. 103(c) is strictly limited to subject matter that A) qualifies as prior art only under 35 U.S.C. 102(f) or 35

U.S.C. 102(g), and B) was commonly owned with the claimed invention at the time the invention was made". Therefore, the subject matter of Takemura is not disqualified as prior art.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
March 30, 2010

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815